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| APPLICATION NO.                                                                                             | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-------------------------------------------------------------------------------------------------------------|-------------|----------------------|---------------------|------------------|
| 10/699,390                                                                                                  | 10/31/2003  | Yung-Hung Chen       | 250606-1010         | 3274             |
| 24504                                                                                                       | 7590        | 01/31/2005           | EXAMINER            |                  |
| THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP<br>100 GALLERIA PARKWAY, NW<br>STE 1750<br>ATLANTA, GA 30339-5948 |             |                      | TRA, ANH QUAN       |                  |
|                                                                                                             |             |                      | ART UNIT            | PAPER NUMBER     |
|                                                                                                             |             |                      | 2816                |                  |

DATE MAILED: 01/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/699,390

Applicant(s)

CHEN, YUNG-HUNG

Examiner

Quan Tra

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10 December 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 12-14 is/are rejected.
- 7) ☒ Claim(s) 10 and 11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

This office action is in response to the amendment filed 12/10/04. A new ground of rejection is introduced.

#### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 is indefinite because there is no antecedent basis for the limitation “the differential amplifier”.

Claim 9 is misdescriptive and rendered the claim indefinite. It is misdescriptive to recite “the MOS transistor is PMOS transistor”. Claim 6 recites that the source of the MOS transistor is connected to ground. Therefore, according to the drawings, the MOS must be NMOS, not PMOS.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Art Unit: 2816

4. Claims 1-3, 5, 8, 9, 12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim (USP 67778007).

As to claim 1, Lim discloses in figure 7 a voltage reference generator for generating an output voltage (VINT) at an output node, comprising: a level shifter (P4, P3) for shifting a first reference voltage (voltage at the gate of P4) into the output voltage at the output node according to a shift between the first reference voltage and the output voltage; and a feedback circuit (10) for monitoring the output voltage and a second reference voltage (VREF) to control the shift and to normalize the output and second reference voltages.

As to claim 2, figure 7 shows that the level shifter includes a source follower (P4) coupled between a voltage source (ground) and the output node, the source follower having an input node (gate) for receiving the first reference voltage.

As to claim 3, figure 7 shows that the source follower has an MOS transistor having a drain connected to the voltage source, a source as the output node and a gate at the input node, and further having a current source (P3) controlled by the feedback circuit and connected to the source of the MOS transistor.

As to claim 5, figure 7 MOS transistor is a PMOS transistor.

As to claim 8, figure 10 shows that the MOS transistor is a NMOS transistor.

Insofar as understood to claim 9, figure 7 shows the MOS transistor P3 is an PMOS transistor.

As to claim 12, figure 7 shows that the feedback circuit has a differential amplifier with an inverted input, a non-inverted input and an output, the non-inverted input coupled to the

Art Unit: 2816

output node, the inverted input coupled to the second reference voltage, and the output coupled to a current source (P3) in the level shifter to control the shift of the level.

As to claim 14, figure 7 shows a voltage divider (R4, R6) to provide the first reference voltage (at the gate of P4) and a third reference voltage (voltage at one of the connection nodes of resistors R7 in figures 9A and B).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4, 6, 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (USP 67778007) in view of Khalid (US 20040150464) (previously cited).

As to claim 4, Lim's figure 7 shows all limitations of the claim except for the MOS transistor is a NMOS transistor. However, Khalid's figure 1 shows two voltage generator circuits having opposite structure that capable of generating the same reference voltage. Therefore, it would have been obvious to one having ordinary skill in the art to reverse the structure of Lim's figure 7 by reversing the transistor types and the power supplies due doctrine function equivalent. Thus, the modified Lim's figure 7 shows the MOS transistor is NMOS transistor.

As to claim 6, the modified Lim's figure 7 shows that the current source (P3) (P3 now is an NMOS transistor) is an MOS transistor having a drain connected to the output node, a source connected to a ground, and a gate connected to the output of the differential amplifier.

Art Unit: 2816

As to claim 7, the modified Lim's figure 7 shows a constant current source (IL) coupled between the output node and another voltage source.

As to claim 13, Lim's figure 10 shows all limitations of the claim except for a low-pass filter connected between output of the differential amplifier and current source in the level shifter. However, Khalid's figure 1B shows a low-pass filter 12 coupled to the output of differential amplifier 11 and to the gate of current source 13 in order to filter the output voltage of the amplifier 11. Therefore, it would have been obvious to one having ordinary skill in the art to add a low-pass filter to the output of Lim's differential amplifier for the purpose of filtering the output of the amplifier.

#### ***Allowable Subject Matter***

7. Claims 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10 and 11 would be allowable because the prior art fails to teach or suggest a low-pass filter to filter out a high frequency portion of the first reference voltage and direct the first reference voltage to the level shifter.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Quan Tra', with a stylized, flowing script.

Quan Tra  
Primary Examiner

January 27, 2005